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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
09/164,216	09/30/98	PASQUALINI	R	NSC1-D8400

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EXAMINER	
NADAV,O	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/15/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

Office Action Summary	Application No. 09/164,216	Applicant(s) Pasqualini
	Examiner ORI NADAV	Group Art Unit 2811

☒ Responsive to communication(s) filed on *Apr 12, 2000*.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-11 and 15-31* is/are pending in the application.

Of the above, claim(s) *4, 7, 8, and 24-31* is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-3, 5, 6, 9-11, and 15-23* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *2*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Election/Restriction

1. Applicant's election of claims 1, 2-3, 5-6, 9-11 and 15-23 in Paper No. 9 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Objections

2. Claim 16 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The structural limitation of a plurality of second floating lateral clamp diodes being connected to a positive line, as recited in dependent claim 16, is also recited in parent claim 15.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 3 and 18 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

5. There is no support in the specification for a second region of a second conductivity type encircling a well of a second conductivity type, as recited in claims 3 and 18. Applicant recites a well encircling a second region of a second conductivity type.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 9, 11 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is impossible for a third region to be formed in a first region, and yet to encircle the first region, as recited in claims 11 and 21.

8. Claim 9 is a dependent claim of a non-elected claim, thus rendering it indefinite.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 5 and 12-14, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gens et al. (5,515,225).

Gens et al. teach in figure 2 a semiconductor chip having a substrate (figure 4, the external line encircling R1) of a first conductivity type, the chip comprising: a pad P2, an ESD positive line R1 not being connected to a voltage source, an ESD negative ring R2, and a plurality of floating lateral clamp diodes (column 3, lines 48-49) connected to the pad so that first and second floating lateral clamp diodes are connected to the pad and the positive and negative lines, respectively. Although Gens et al. do not explicitly disclose a positive line R1 not being connected to a voltage source, it is clear from figure 2 and since R1 is floating that positive line R1 is not connected to a voltage source. Therefore, the claimed structure is considered to be in at least obvious over Gens et al.

Regarding claim 5, Gens et al. teach in figure 4 a negative line encircling the periphery of the chip.

Regarding claims 12-13, Gens et al. teach floating ESD positive and negative rings connected package pins (column 2, line 43).

11. Claims 2-3 and 10-11, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gens et al. in view of Rao et al. (5,770,886).
Gens et al. teach in figure 2 substantially the entire claimed structure, as applied to claim 1 above, except disclosing the structure of the floating diode.
Rao et al. teach in figure 2 a diode 11 formed in a well of a second conductivity type 26, wherein plurality of spaced apart first regions of the first conductivity type 35, 36 being electrically connected together, and a second region of the second conductivity type 42 being formed in the well and having dopant concentration higher than that of the well.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the floating diodes in Gens et al.'s device in a well, as taught by Rao et al., because it is well known in the art to form floating devices including diodes in a well in order to provide electrical isolation to the devices.

Regarding claim 11, Rao et al. teach in figures 7 and 9 a third region of a second conductivity type 108 encircling the well 111, and having a dopant concentration greater than that of the well.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a third region of a second conductivity type encircling the well, and having a dopant concentration greater than that of the well in order to provide better isolation to floating diodes.

12. Claims 6, 9, 15-16, 19 and 22-23, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gens et al. in view of Admitted Prior Art (APA).

Gens et al. teach in figure 2 a semiconductor chip having a substrate (figure 4, the external line encircling R1) of a first conductivity type, the chip comprising: a plurality of pads P1, P2, an ESD positive line R1, an ESD negative ring R2, and a plurality of floating lateral clamp diodes (column 3, lines 48-49) connected to the pad so that each first and second floating lateral clamp diodes is connected to the pad and the positive and negative lines, respectively.

Gens et al. do not teach a plurality of ESD positive lines and plurality of ESD switches connected to the positive line and the negative ring, respectively.

APA teaches in figure 5 a plurality of ESD positive lines (page 12, lines 8-13), and plurality of ESD switches connected to the positive line and to the negative ring, respectively (page 2, lines 24-27).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to connect plurality of ESD switches to plurality of positive lines and to the negative ring,

respectively, in Gens et al.'s device, because it is conventional to connect plurality of ESD switches between plurality of positive lines and the negative ring in order to provide effective unidirectional flow of current during ESD operation.

Regarding claims 9, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the ESD switches between two adjacent corners of the chip, since the location of the switch on the chip is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization regarding the operation of the device.
Regarding claim 19, Gens et al. teach in figure 4 a negative line encircling the periphery of the chip.

Regarding claims 12-23, Gens et al. teach floating ESD positive and negative rings connected package pins (column 2, line 43).

13. Claims 17-18 and 20-21, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gens et al. and Admitted Prior Art (APA), as applied to claim 15 above, and further in view of Rao et al.
Gens et al. and APA teach substantially the entire claimed structure, as applied to claim 15 above, except disclosing the structure of the floating diode.

Rao et al. teach in figure 2 a diode 11 formed in a well of a second conductivity type 26, wherein plurality of spaced apart first regions of the first conductivity type 35, 36 being electrically connected together, and a second region of the second conductivity type 42 being formed in the well and having dopant concentration higher than that of the well.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the floating diodes in Gens et al.'s device in a well, as taught by Rao et al., because it is well known in the art to form floating devices including diodes in a well in order to provide electrical isolation to the devices.

Regarding claim 21, Rao et al. teach in figures 7 and 9 a third region of a second conductivity type 108 encircling the well 111, and having a dopant concentration greater than that of the well.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a third region of a second conductivity type encircling the well, and having a dopant concentration greater than that of the well in order to provide better isolation to floating diodes.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group

2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Tom Thomas
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Ori Nadav, Ph.D.

May 8, 2000